SIDDHARTH INSTITUTE OF ENGINEERING &TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
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QUESTION BANK (DESCRIPTIVE)

Subject with Code: Switching Theory and Logic Design (20EC0403) **Course & Branch:** B.Tech& ECE

Year &Sem: II-B.Tech& I-Sem **Regulation:** R20

UNIT-I
BOOLEAN ALGEBRA AND LOGIC GATES

1.	State and prove any 4 Boolean theorems with examples.	[L3][CO1]	[12M]
2.	State and prove the following Boolean laws: (i).Commutative (ii).Associative (iii).Distributive	[L3][CO1]	[12M]
3.	a) State and Prove Demorgan's Theorem using suitable example.	[L3][CO1]	[6M]
	b)Simplify to a sum of 3 terms: A'C'D' +AC' +BCD + A'CD' + A'BC + AB'C'	[L4][CO2]	[6M]
4.	Simplify the following Boolean expressions. i.A'C'+ABC +AC' to three literals ii.(X'Y' + Z)' + Z + XY + WZ to three literals. iii.A'B(D' + C'D) + B(A +A'CD) to one literal. iv.(A'+C)(A'+C')(A +B+C'D)to four literals.	[L4][CO2]	[12M]
5.	a)Simplify the following Boolean functions to minimum number of literals: i.(a + b)' (a' + b')' ii.y(wz' + wz) + xy	[L4][CO2]	[6M]
	b)State and prove Boolean laws related to OR, AND, NOT gates.	[L3][CO1]	[6M]
6.	Identify the Dual of the following Boolean expressions (i) AB'C+AB'D+A'B' (ii) A'B'C+ABC'+A'B'C'D	[L2][CO2]	[12M]
7.	Express the complement of the following Boolean expressions. i.B'C'D + (B + C + D)' + B 'C'D'E ii.AB + (AC)' + (AB + C) iii.A'B'C' + A'BC' + AB'C' + ABC' iv.AB + (AC)' + AB'C	[L2][CO2]	[12M]
8.	a) Express the following functions in sum of Minterms and product of Maxterms. i.F (A,B,C,D) = B'D + A'D + BD ii.F(x,y,z) = (xy + z)(xz+y)	[L2][CO2]	[6M]
	b).Express the following Boolean functions in to Canonical form: i. F=AB+BC+CA ii. F= XY+Z+YZ+XYZ	[L2][CO1]	[6M]
9.	For the given Boolean function F=XY'Z + X'Y'Z +W'XY + WX'Y + WXY		
	a) Simplify the function to minimal literals using Boolean algebra	[L4][CO2]	[6M]
	b). Draw the logic diagramfor the simplified expression of the above using AOI.	[L1][CO2]	[6M]
10	Describe about the digital logic gates	[L1][CO1]	[12M]

UNIT –II
GATE – LEVEL MINIMIZATION

1.	a) List the steps involved in simplification of K map.	[L1][CO1]	[4M]
	b) Simplify the following expression using the K-map for the 3-variable and draw the logic diagram using AOI. Y = AB'C+A'BC+A'B'C+A'B'C'+AB'C'	[L4][CO3]	[8M]
2.	a)Simplify the Boolean expression using K-map and draw the logic diagram using AOI. F=A'+AB+ABD'+AB'D'+C'	[L4][CO2]	[6M]
	b)Simplify the Boolean function using 5 variable K-map. F=∑m(0, 1,2, 4, 7, 8, 12, 14, 15, 16, 17, 18, 20, 24, 28, 30, 31)	[L4][CO2]	[6M]
3.	Apply the K-Map technique to simplify the Boolean expression in POS and SOP form using K-map F(A,B,C,D) = Σ(1,2,4,5,9,12,13,14)	[L4][CO2]	[12M]
4.	a) Simplify the following Boolean function for minimal POS form using K-map F(X,Y,Z) = X'YZ + XY'Z' + XYZ + XYZ'	[L4][CO2]	[6M]
	b) Simplify the Boolean function Using K-Map F(A,B,C,D)=∑(1,3,7,11,15)+d(0,2,5)	[L4][CO3]	[6M]
5.	a) Simplify using K-map and express the reduced expression in SOP and POS form. F = Σ m (0, 6, 8, 13, 14) + Σ d (2 , 4, 10)	[L4][CO2]	[6M]
	b) Implement the following Boolean function using NAND and NOR gates. Y=(AB'+A'B)(C+D').	[L4][CO3]	[6M]
6.	Simplify the following expressions using K-Map and realize with NAND and NOR gates. F = πM (1, 2, 3, 8, 9, 10, 11, 14). πd (7,15)	[L4][CO3]	[12M]
7.	Simplify the following expressions using K-Map and realize with NAND and NOR gates. F = ∑m (0,2,5,9,15) + ∑d(6,7,8,10,12,13)	[L4][CO3]	[12M]
8.	Apply the K-Map technique to simplify the Boolean expression and realize with NAND and NOR gates. F = AB'C + A'B'C + A'BC +AB'C' + A'B'C'.	[L3][CO3]	[12M]
9.	Deduce the following Boolean expressions using K-map and implement them using NAND and NOR gates: (i) F (W, X, Y, Z) =W'X'YZ' + W'XYZ' + WX'YZ' + WX'YZ+WXYZ'+WXYZ	[L4][CO3]	[6M]
	b) Explain the structure of Ex-OR gate by K-Map using 4 Variable.	[L2][CO2]	[6M]
10.	Simplify the following Boolean function using Tabulation method, realize with NAND gates and NOR gates. Y(A, B,C,D) = Σ(1,3,5,8,9,11,15)	[L4][CO2]	[12M]

UNIT –III
COMBINATIONAL LOGIC

1	a) Define Combinational Circuit, explain the analysis procedure of a combinational logic circuit using suitable example.	[L2][CO1]	[6M]
	b) Design & implement BCD to Excess-3 code converter.	[L3][CO4]	[6M]

2	a) Design & implement a 4-bit Binary-To-Gray code converter.	[L3][CO4]	[6M]
	b) Design a 4 bit binary-to-BCD code converter	[L3][CO4]	[6M]
3	a) Design & implement Full Adder with truth table.	[L3][CO5]	[6M]
	b) Design & implement Full Subtractor with truth table.	[L3][CO5]	[6M]
4	a) Design a 4 bit parallel adder/ Subtractor using full adders	[L3][CO3]	[6M]
	b) Construct a Decimal Adder-circuit.	[L3][CO3]	[6M]
5	Explain Binary Multiplier with an example.	[L2][CO3]	[12M]
6	a) Define Magnitude comparator, Implement a 2-bit Magnitude comparator and write down its design procedure and applications.	[L3][CO3]	[6M]
	b) Design & implement Full Adder using Decoder.	[L3][CO4]	[6M]
7	a)What is Decoder? Explain a 2 to 4 line binary decoder.	[L2][CO5]	[6M]
	b)Draw the circuit for 3:8 decoder and explain	[L2][CO5]	[6M]
8	a)Implement the following Boolean functions using decoder and ORgates:F1(A,B,C,D)=∑(2,4,7,9) F2(A,B,C,D)= ∑(10,13,14,15)	[L3][CO4]	[6M]
	b) What is encoder? Design octal to binary encoder.	[L3][CO3]	[6M]
9	a) What is multiplexer? Construct 4:1 multiplexer with logic gates and truth table .	[L3][CO4]	[6M]
	b) Implement the following Boolean function using 8:1 multiplexer. F(A,B,C,D) = A'BD'+ACD+B'CD+A'C'D.	[L3][CO4]	[6M]
10	a)What is Demultiplexer? Design 1:8 demultiplexer using two 1:4 demultiplexer.	[L3][CO4]	[6M]
	b) Design 32:1 Mux using two 16:1 MUXs and one 2:1 MUX.	[L3][CO4]	[6M]

UNIT –IV
SYNCHRONOUS SEQUENTIAL LOGIC

1.	a) What is sequential circuit? Explain with the helpofablockdiagram.	[L2][CO1]	[4M]
	b) Differentiate in between combination and sequential circuits.	[L2][CO1]	[4M]
	c) Differentiate in between synchronous and asynchronous sequential circuits.	[L2][CO1]	[4M]
2.	a) Define Latch? What are the different types of Latches?	[L1][CO1]	[4M]
	b) Define Flip-Flop? What are the different types of Flip-Flops?	[L1][CO1]	[4M]

	c) Explain the working principle of RS Flip-Flop in detail.	[L1][CO2]	[4M]
3.	a) Explain the working principle of D & T Flip-Flops.	[L2][CO2]	[6M]
	b) Explain the working principle of JK Flip-Flop in detail.	[L2][CO2]	[6M]
4.	a) Derive the characteristic equations for D & T Flip-Flops.	[L3][CO5]	[6M]
	b) Convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram.	[L2][CO4]	[6M]
5.	a) Design T Flip Flop by using JK Flip Flop and explain the logic diagram.	[L3][CO5]	[6M]
	b) Analyze the clocked sequential circuits.	[L4][CO1]	[6M]
6.	Explain in brief about various types of shift registers	[L2][CO3]	[12M]
7.	Design a 4 bit decade counter	[L4][CO5]	[6M]
8.	a) Define counter and design a 4-bit Ripple counter	[L4][CO5]	[8M]
	b) Explain in brief about a 2-bit synchronous up-counter.	[L4][CO5]	[4M]
9.	What is a synchronous counter? Design a 3-bit synchronous up/down counter.	[L4][CO5]	[12M]
10.	Explain about the following counters a)Ring counter b)Johnson counter	[L2][CO5]	[12M]

UNIT –V

UNIT-V FINITE STATE MACHINES AND PROGRAMMABLE MEMORIES

1.	a) Define melay model? Explain it with neat diagram.	[L1][CO1]	[4M]
	b) Define moore model. Explain it with neat diagram.	[L1][CO1]	[4M]
	c) Distinguish between melay & moore machines	[L2][CO1]	[4M]
2.	Explain the following related to sequential circuits with suitable examples a) State diagram b) State table c) State assignment	[L2][CO1]	[12M]
3.	Derive the simplified sequential circuit for the following state table.	[L3][CO6]	[12M]

PS	Next State	Output

			X=0	X=1	X=0	X=1		
		A	a	b	0	0		
		ban	c	d	0	0		
		c	a	d	0	0		
		d	e	f	0	1		
		e	a	f	0	1		
		f	g	f	0	1		
		g	a	f	0	1		
4.	Determine the minimal state equivalent of the state table given.						[L3][CO6]	[12M]
		PS	Next State		Output			
			X=0	X=1	X=0	X=1		
		a	a	b	0	0		
		b	c	g	0	1		
		c	a	d	0	0		
		d	e	f	0	1		
		e	c	g	0	1		
		f	a	b	0	0		
		g	E	f	0	1		
5.	Explain in brief about Programmable Read Only Memory (PROM) with suitable example.						[L2][CO2]	[12M]
6.	a) Compare ROM and RAM.						[L2][CO1]	[6M]
	b) Classify various types of RAMs						[L2][CO1]	[6M]
7.	Illustrate the PLA for the following Boolean function (i)F1= Σm(0,1,3,4) (ii)F2 = Σm(0,1,2,3,4,5).						[L3][CO5]	[12M]
8.	Illustrate the PLA for the following Boolean function F1(A,B,C)= Σm(3,5,7)F2(A,B,C)= Σm(4,5, 7).						[L3][CO5]	[12M]
9.	Illustrate the PAL for the following Boolean function (i)F(A,B,C,D) = Σm(2,3,8,9,,10,12,13) (ii)G(A,B,C,D) = Σm(1,3,4,6,9,12,14)						[L3][CO5]	[12M]
10.	Illustrate the PAL for the following Boolean function (i)A(w,x,y,z) = Σm(0,2,6,7,8,9,12,13) (ii)B(w,x,y,z)) = Σm(0,2,6,7,8,9,12,13,14)						[L3][CO5]	[12M]